Uncooled Digital IRFPAs Based on Microbolometers for Thermal Imaging Applications

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IR-detectors (IRFPA = infrared focal plane array) in the LWIR (8 .. 14 µm) are divided into cooled and uncooled detectors. Cooled IR-detectors typically achieve a better thermal resolution (lower NETD) at higher cost due to the need of a Stirling cooler resulting in higher power dissipation, higher weight, and larger volume compared to uncooled IR-detectors. Uncooled IR-detectors operate at ambient temperature and dominate the low-cost commercial and portable market for thermal imaging applications without the drawbacks of cooled IR-detectors with a slightly larger NETD. The IRFPA consists of an array of microbolometer as the IR-sensorelement, a CMOS readout circuitry for converting the thermal signal into a digital signal, and a vacuum package. The IRFPAs are typically fabricated 8" CMOS wafers with an additional surface micromachining process. Typical applications for IRFPAs are thermal imaging, pedestrian detection for automotive driving-assistance systems, fire fighting, biological imaging, or military applications like target recognition.

For the detection of LWIR-radiation a resistive microbolometer using amorphous silicon or vanadium oxide as the sensing layer is realized (**Fig. 1**). A micromachined membrane is suspended approximately 2 µm above a metal reflector on top of a planarized CMOS and absorbs the IR-radiation. The resulting interferometric structure is optimized for maximum absorption in the FIR band. At the corners, the metal vias connecting the substrate to the membrane are placed. Two thermal insulating legs are defined along the edges of the membrane. Currently most of the fabricated microbolometers exhibit a pixel pitch of 17 µm. In the future the pixel pitch will be scaled down to 12 µm to enlarge the optical format and for a price reduction.

A vacuum package with an integrated infrared transparent window is required for uncooled IRFPAs based on microbolometers to reduce thermal losses by gas conduction. The most significant packaging trend for reducing packaging costs is the realization of wafer-level-packages (WLP). Fraunhofer IMS uses a chip scale package (**Fig. 2**) as a special WLP. The chip-scale package consists of the substrate, which includes the ROIC and the microbolometer array. A solder frame fabricated by a standard patterned electrochemical deposition (ECD) process surrounds the microbolometer. The IR-transparent lid consists of silicon and therefore causes lower mechanical stress due to equal expansion coefficient between the lid and the substrate. The second advantage of silicon is the lower production costs compared to germanium lids. The transmission is increased by a double-sided antireflection coating. During a flip chip process the lid is precisely placed on top of the substrate. The final process step in the fabrication of a chip scale package is the soldering under vacuum. For thermal imaging applications the chip-scale-package is placed on a detector board by a chip-on-board technique. This detector board provides all necessary electrical and mechanical interfaces (**Fig. 5**).

Fraunhofer IMS has developed an innovative digital QVGA-IRFPA (**Fig. 3**) with an optical resolution of QVGA (320 x 240 pixel). The microbolometers are read out by using a novel readout architecture which utilizes massively parallel Sigma-Delta-ADCs (ΣΔ-ADCs) located under the array. The ROICs are completely fabricated at Fraunhofer IMS in a 0.35 µm CMOS technology on 8'' wafers (**Fig. 4**). The digital QVGA-IRFPA is electro-optically characterized by using black bodies as radiation sources in by an automatic test system. The histogram of

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the NETD value shows a mean value of $NETD_{mean}$ = 73.2 mK (**Fig. 6**). An uncompensated FIR image of a digital QVGA-IRFPA shows the temperature distribution of a face (**Fig. 7**).

Figures

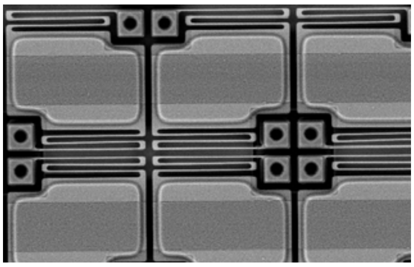

Fig. 1 SEM micrograph of a bolometer (left: top view)

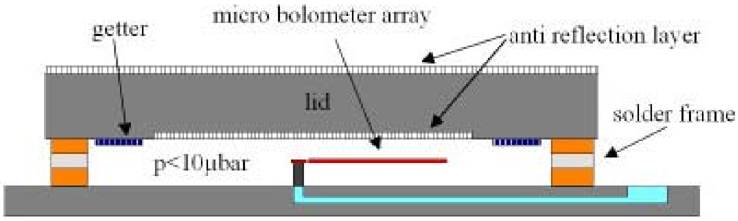

Fig. 2 Principle of a chip-scale vacuum package

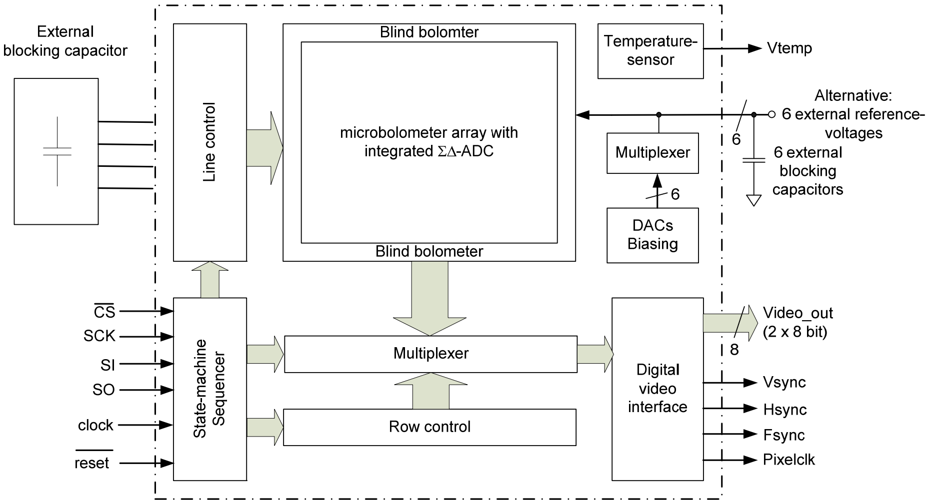

Fig. 3 Block diagram ROIC of digital QVGA-IRFPA

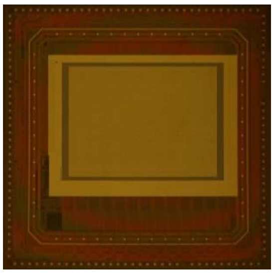

Fig. 4 Chip photo digital QVGA-IRFPA

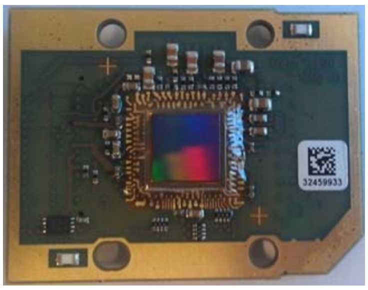

Fig. 5 Realization of the detector board

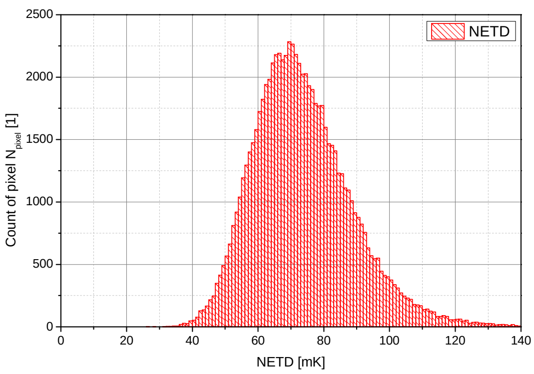

Fig. 6 Noise equivalent temperature difference NETD

Fig. 7 Uncompensated FIR image