Wafer Level System Integration and 3D Packaging

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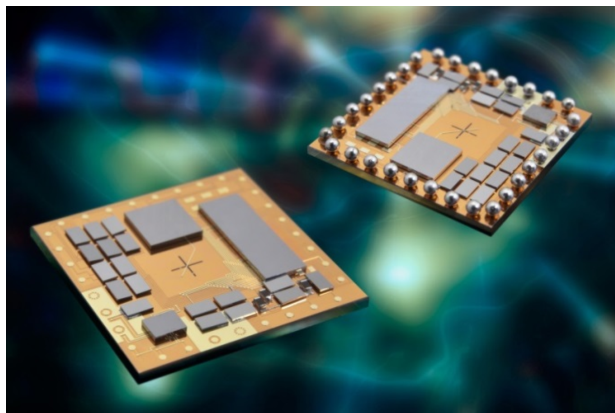
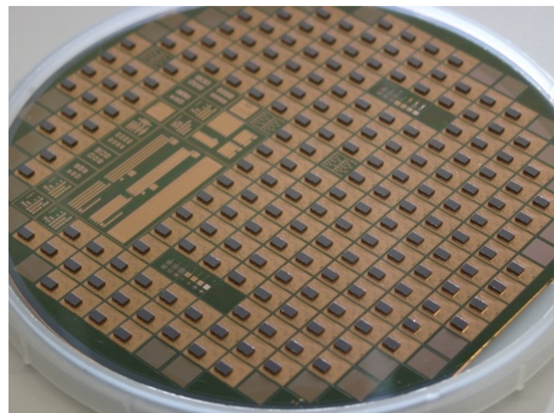
Wafer Level packaging and 3D integration belong to the most important key technologies for microelectronics to meet the growing demands regarding more functionality, increase in performance, miniaturization and cost reduction and becomes important for application areas e.g. cyber physical systems, internet of things, ambient assisted living (AAL), information & communication, security and health. Interposers with Through Silicon Vias (TSVs) are becoming a very important element and a key enabler for the realization of 3D Systems-in-Packages (SiPs) whose main advantages are the decoupling of front end / back end processing for the implementation of TSVs and redistribution layers. Different applications result in different technical approaches ranging from high density TSV integration, high density RDL for digital applications to interposers for RF applications as well as MEMS and sensor integration and optical interconnects.

The advantages of vertical integration include:

- Improved electrical performance thanks to the faster signal speeds and higher bandwidth resulting from shorter and narrower signal paths
- Cost reduction through partitioning of large and expensive chip components
- Increased functionality due to heterogeneous integration of components, which are fabricated using different technology nodes
- Smaller form factor and easy access to sensitive surfaces for sensor applications thanks to backside contacts
- Increased optical fill factor for large-area multi-sensor applications
- Reduction of process time thanks to parallelization of production processes

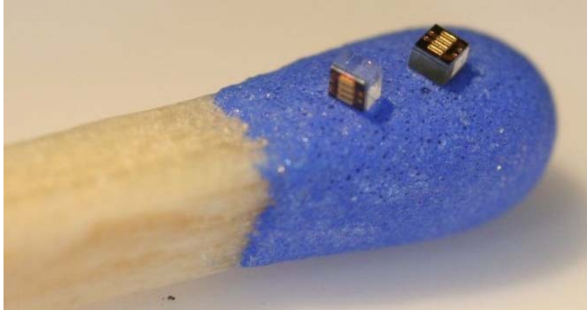


24 GHz module on glass
BCB – Cu multilayer

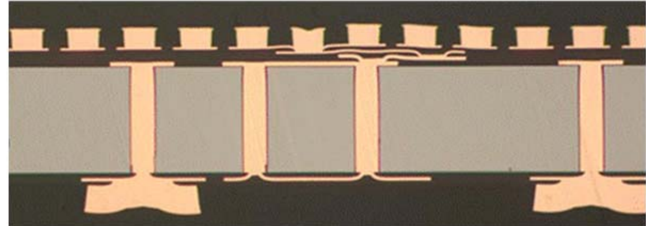


Wafer Level Assembly on
RDL Wafer

Fraunhofer IZM’s activities include concept and process development, characterization, reliability assessment and prototyping of 3D systems. Our labs are equipped for all processes involved in TSV manufacture and subsequent packaging. We have built up, assembled and characterized (electrically and thermo-mechanically) a wide range of 3D systems for different applications, such as image sensors, logic, MEMS, silicon and glass interposers, in a number of different completed and ongoing projects.



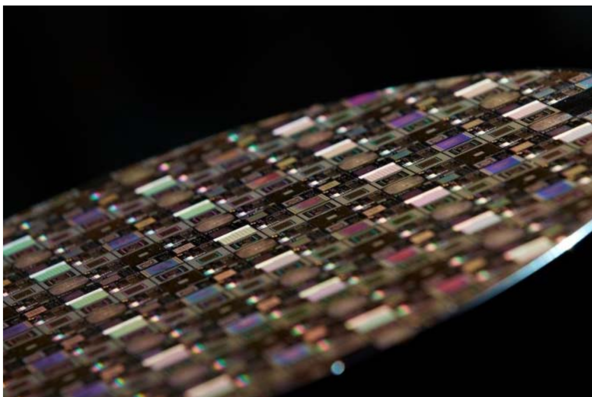
Wafer-Level-Cameras



Silicon Interposer with
Through Silicon Vias (TSVs)

Trends - The research and development goals are aligned to the following:

- Evaluation and implementation of new material e.g. polymeric dielectric (< 200°C curing)
- Development and realization of adapted fine-pich interconnect structures (micro bumps, Cu-Pillar, Cu-Cu) on chip/substrate level
- Development of new interconnect structures and systems (low temperatures, low force) for ultra-thin chips and wafer bonds
- BeOL-compatible TSV integration (via middle) for 3D systems
- Adapted pre-assembly technologies (wafer thinning/ dicing) and thin wafer handling processes
- Development of highly reliable manufacturing-compatible 3D assembly technologies (D2W/W2W)



Silicon Interposer Wafer